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<u>L24</u>	L23 and pipelin\$ near4 (modif\$ or chang\$ or alter)	1	<u>L24</u>
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1 [Compiler-based I/O prefetching for out-of-core applications](#)



Angela Demke Brown, Todd C. Mowry, Orran Krieger

 May 2001 **ACM Transactions on Computer Systems (TOCS)**, Volume 19 Issue 2

Publisher: ACM Press

 Full text available: [pdf\(499.03 KB\)](#)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Current operating systems offer poor performance when a numeric application's working set does not fit in main memory. As a result, programmers who wish to solve "out-of-core" problems efficiently are typically faced with the onerous task of rewriting an application to use explicit I/O operations (e.g., read/write). In this paper, we propose and evaluate a fully automatic technique which liberates the programmer from this task, provides high performance and requires only minima ...

Keywords: compiler optimization, prefetching, virtual memory

2 [Exploiting fine-grain thread level parallelism on the MIT multi-ALU processor](#)



Stephen W. Keckler, William J. Dally, Daniel Maskit, Nicholas P. Carter, Andrew Chang, Whay S. Lee

 April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture ISCA '98**, Volume 26 Issue 3

Publisher: IEEE Computer Society, ACM Press

 Full text available: [pdf\(1.56 MB\)](#)

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Much of the improvement in computer performance over the last twenty years has come from faster transistors and architectural advances that increase parallelism. Historically, parallelism has been exploited either at the instruction level with a grain-size of a single instruction or by partitioning applications into coarse threads with grain-sizes of thousands of instructions. Fine-grain threads fill the parallelism gap between these extremes by enabling tasks with run lengths as small as 20 cyc ...

3 [Processor-memory coexploration using an architecture description language](#)



Prabhat Mishra, Mahesh Mamidipaka, Nikil Dutt

 February 2004 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 3 Issue 1


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IEEE JNL. IEEE Journal or Magazine

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Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM Inte
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1 [On parallel execution of multiple pipelined hash joins](#)



Hui-I Hsiao, Ming-Syan Chen, Philip S. Yu

 May 1994 **ACM SIGMOD Record , Proceedings of the 1994 ACM SIGMOD international conference on Management of data SIGMOD '94**, Volume 23 Issue 2

Publisher: ACM Press

Full text available: pdf(1.24 MB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this paper we study parallel execution of multiple pipelined hash joins. Specifically, we deal with two issues, processor allocation and the use of hash filters, to improve parallel execution of hash joins. We first present a scheme to transform a bushy execution tree to an allocation tree, where each node denotes a pipeline. Then, processors are allocated to the nodes in the allocation tree based on the concept of synchronous execution time such that inner relations (i.e., hash tables) ...

2 [Co-synthesis of pipelined structures and instruction reordering constraints for instruction set processors](#)



Ing-Jer Huang

 January 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 1

Publisher: ACM Press

Full text available: pdf(1.58 MB)

 Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents a hardware/software co-synthesis approach to pipelined ISP (instruction set processor) design. The approach synthesizes the pipeline structure from a given instruction set architecture (behavioral) specification. In addition, it generates a set of reordering constraints that guides the compiler back-end (reorderer) to properly schedule instructions so that possible pipeline hazards are avoided and throughput is improved. Co-synthesis takes place while resolving ...

Keywords: compiler instruction optimization\, instruction set processor, pipeline hazards, pipeline taxonomy, synthesis

3 [Pipeline Architecture](#)



C. V. Ramamoorthy, H. F. Li

 January 1977 **ACM Computing Surveys (CSUR)**, Volume 9 Issue 1